Short Channel MOS Transistor

Professor Chris H. Kim

University of Minnesota
Dept. of ECE

chriskim@umn.edu
www.umn.edu/~chriskim/

Remember the Standard V_t Equation?

$$V_t = V_{fb} + |2\psi_B| + \frac{\sqrt{2qN_a\varepsilon_{si}|2\psi_B|}}{C_{ox}}$$

▪Y. Taur, T. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 2002.

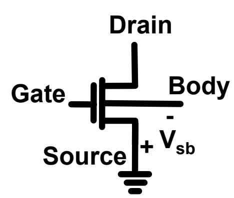
- Detailed derivation given in Taur's book
- Basically, three terms
  - Flat band voltage
  - $2\psi_B$: the magic number for on-set of inversion
  - Oxide voltage

Body Effect (Back Bias)

$$V_{t0} = V_{fb} + |2\psi_B| + \frac{\sqrt{2qN_a\varepsilon_{si}|2\psi_B|}}{C_{ox}}$$

$$V_t = V_{fb} + |2\psi_B + V_{sb}| + \frac{\sqrt{2qN_a\varepsilon_{si}|2\psi_B + V_{sb}|}}{C_{ox}} - V_{sb}$$

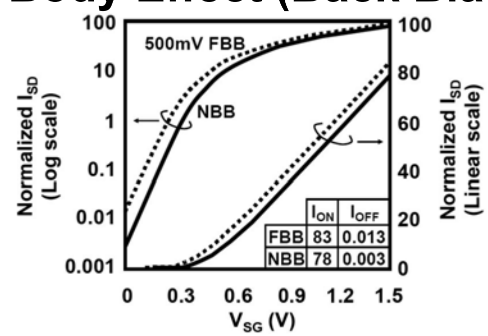
$$V_t = V_{fb} + |2\psi_B| + \frac{\sqrt{2qN_a\varepsilon_{si}|2\psi_B + V_{sb}|}}{C_{ox}}$$



$V_{sb} > 0$: RBB
$V_{sb} < 0$: FBB

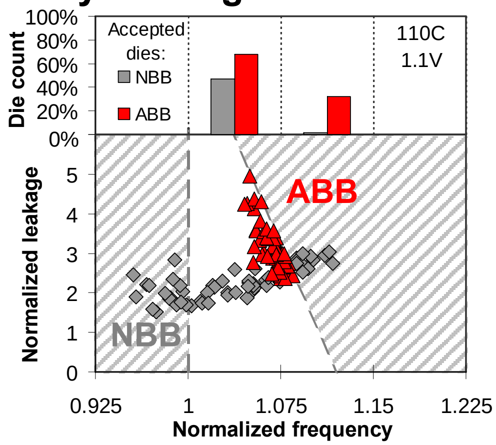
- Body effect degrades transistor stack performance
- However, we need a reasonable body effect for post silicon tuning techniques
- Reverse body biasing, forward body biasing

Body Effect (Back Bias)



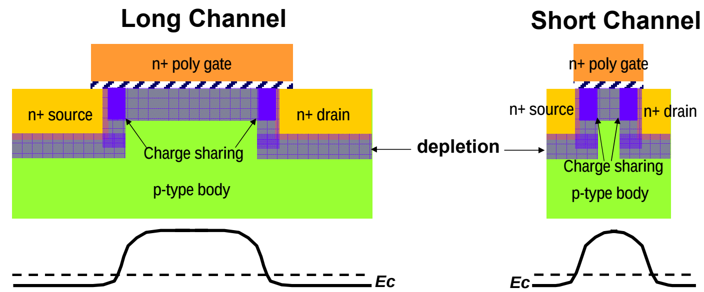
- V_t can be adjusted by applying FBB or RBB
  - Essential for low power and high performance
  - Will talk about body biasing extensively later on

Body Biasing for Process Compensation



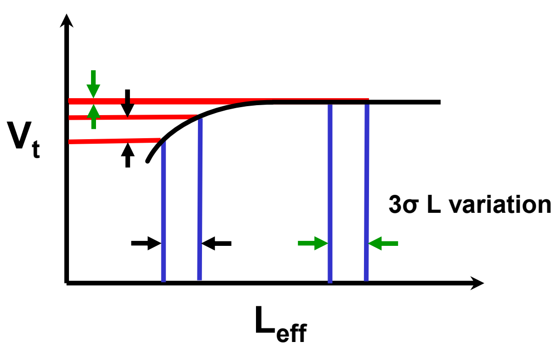
Body bias: controllability to V_t

Short Channel Effect: V_t roll-off



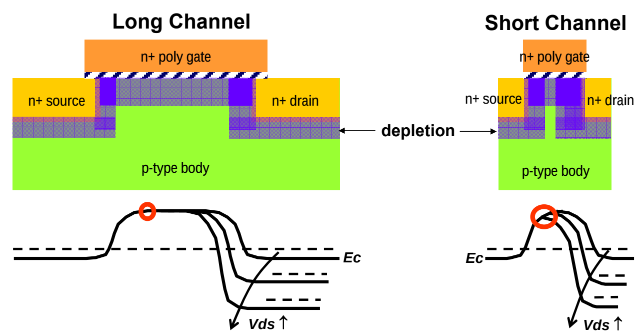
- Ability of gate & body to control channel charge diminishes as L decreases, resulting in Vt-roll-off and body effect reduction

Short Channel Effect: V_t roll-off



- 3σ V_t variation increases in short channel devices

Short Channel Effect: Drain Induced Barrier Lowering (DIBL)



- Increase in V_{DS} reduces V_t and increases V_t-roll-off: DIBL

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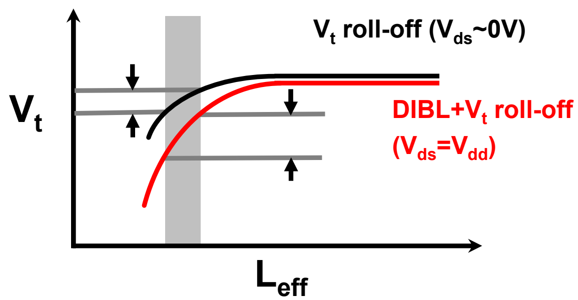
Short Channel Effect: Drain Induced Barrier Lowering (DIBL)



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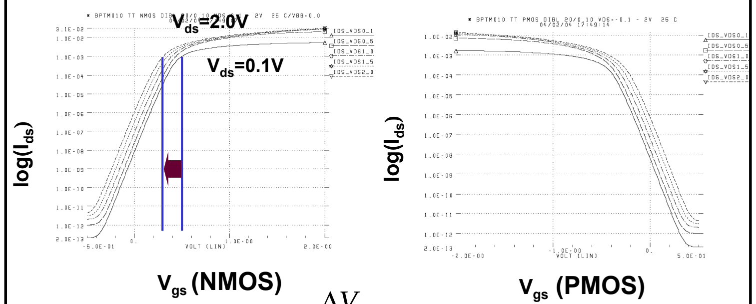
Short Channel Effect: DIBL



- DIBL coefficient $\lambda_d = \frac{\Delta V_t}{\Delta V_{ds}}$
- DIBL increases leakage current
- Dynamic V_{dd} can reduce leakage because of DIBL

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Short Channel V_t Equation

$$V_t = V_{fb} + |2\psi_B| + \frac{\lambda_b}{C_{ox}}\sqrt{2qN_a\varepsilon_s(|2\psi_B| + V_{sb})} - \lambda_d V_{ds}$$

$$V_t = V_{fb} + |2\psi_B| + \frac{\sqrt{2qN_a\varepsilon_{si}|2\psi_B|}}{C_{ox}}$$ (Long channel V_t equation)

[Poon, IEDM, 1973]

$$\lambda_b = 1 - \left(\sqrt{1 + \frac{2W}{X_j}} - 1\right)\frac{X_j}{L}$$

[Ng, TED, 1993]

$$\lambda_d = \left[\frac{L}{2.2\mu m^{-2}(T_{ox} + 0.012\mu m)(W_{sd} + 0.15\mu m)(X_j + 2.9\mu m)}\right]^{-2.7}$$

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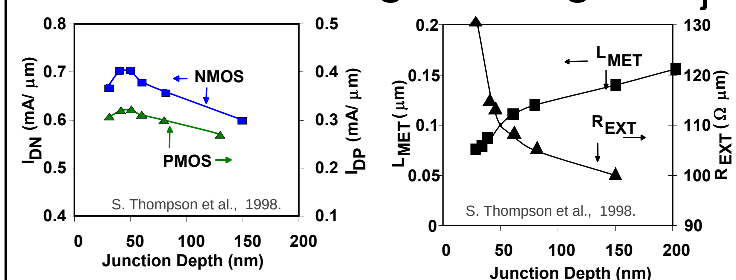
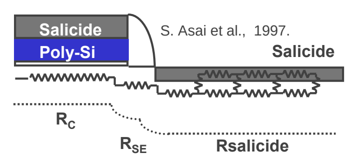
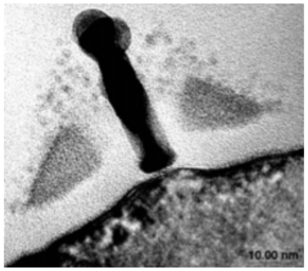
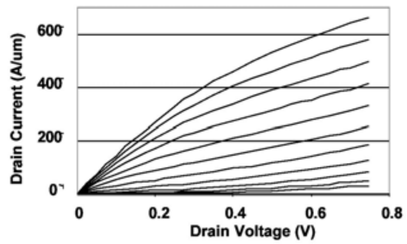
Transistor Scaling Challenges - X_j



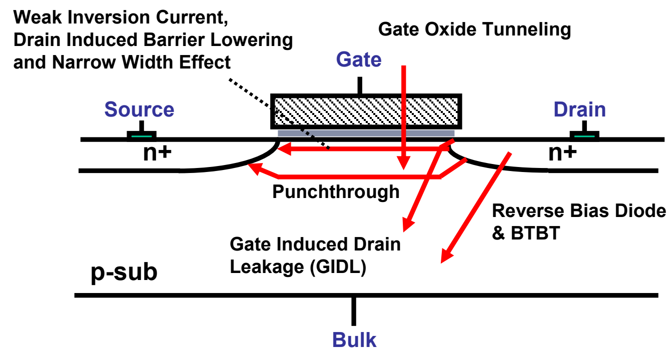


Effect of Series Resistance
(10nm Device)



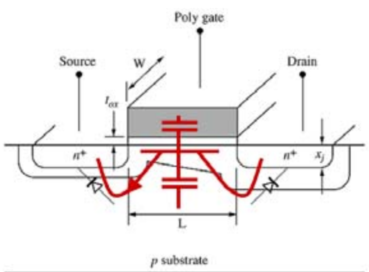


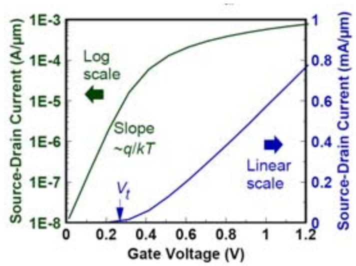
Leakage Components



[Keshavarzi, Roy, and Hawkins, ITC 1997]

Sub-Threshold Current





- **NPN BJT is formed in sub-threshold region**
- **Only difference with a real BJT is that the base voltage is controlled through a capacitive divider, and not directly by a electrode**
- **Like in a BJT, current is exponential to V_{be}**

Sub-Threshold Current

$$I_d = \frac{W}{L}\mu_{eff}C_{ox}\left(\frac{k_BT}{q}\right)^2(m-1)e^{q(V_{gs}-V_t)/mkT}\,(1-e^{-qV_{ds}/kT})$$

Sub-Threshold Swing

$$S = m\frac{kT}{q}\ln 10\ \left({}^{mV}\!/_{dec}\right)\quad , \quad m = 1 + \frac{C_{dep}}{C_{ox}}$$

- Smaller S-swing is better
- Ideal case: m=1 (C_{ox}>>C_{sub})
  - Fundamental limit = 1 * 26mV * ln10 = 60 mV/dec @ RT
  - Can only be achieve by device geometry (FD-SOI)
- Typical case: m≈1.3
  - S = 1.3 * 26mV * ln10 ≈ 80 mV/dec @ RT
  - At worst case temperature (T=110C), S ≈ 100 mV/dec

V_{dd} and V_t Scaling

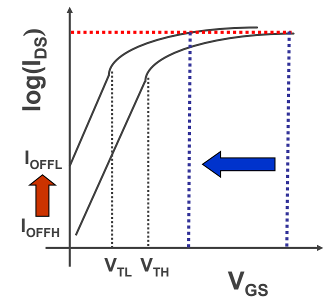
Performance vs Leakage:

$V_T \downarrow$ $I_{OFF} \uparrow$ $I_D(SAT) \uparrow$

$$I_{OFF} \propto \frac{W_{eff}}{L_{eff}} K_1 e^{-V_T/_{mkT/q}}$$

$$I_D(SAT) \propto \frac{W_{eff}}{L_{eff}} K_2 (V_{GS} - V_T)^2$$

$$I_D(SAT) \propto K_3 W_{eff} C_{ox} \upsilon_{SAT} (V_{GS} - V_T)$$



⇨ As V_t decreases, sub-threshold leakage increases

⇨ Leakage is a barrier to voltage scaling

V_{dd} and V_t Scaling

- V_t cannot be scaled indefinitely due to increasing leakage power (constant sub-threshold swing)
- Example

  CMOS device with S=100mV/dec has I_{ds}=10μA/μm @ V_t=500mV

  I_{off}=10μA/μm x 10^{-5} = 0.1 nA/μm

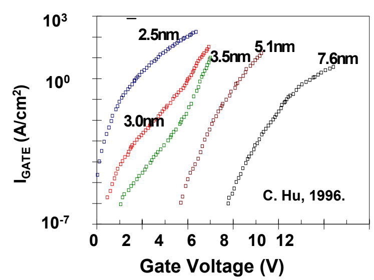
  Now, consider we scale the V_t to 100mV

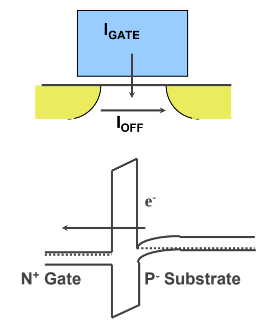
  I_{off}=10μA/μm x 10^{-1} = 1 μA/μm

  Suppose we have 1B transistors of width 1μm

  I_{sub}=1μA/μm x 1B x 1μm = 100 A !!

Gate Oxide Tunneling Leakage





Gate Oxide Tunneling Leakage

- Quantum mechanics tells us that there is a finite probability for electrons to tunnel through oxide
- Probability of tunneling is higher for very thin oxides
- NMOS gate leakage is much larger than PMOS
- Gate leakage has the potential to become one of the main showstoppers in device scaling

$$I_{gate} = AE_{ox}^{2} e^{-B/E_{ox}} \quad , \quad E_{ox} = \frac{V_{dd} - V_t}{t_{ox}}$$

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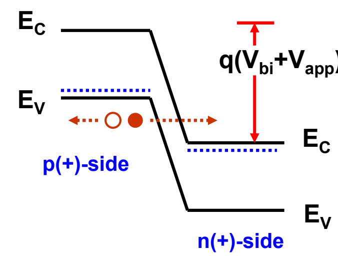
Band-to-Band Tunneling Leakage



S/D junction BTBT Leakage

- Reversed biased diode band-to-band tunneling
  - High junction doping: “Halo” profiles
  - Large electric field and small depletion width at the junctions

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Gate Induced Drain Leakage (GIDL)

- Appears in high E-field region under gate/drain overlap causing deep depletion
- Occurs at low V_g and high V_d bias
- Generates carriers into substrate from surface traps, band-to-band tunneling
- Localized along channel width between gate and drain
- Thinner oxide, higher V_{dd}, lightly-doped drain enhance GIDL
- High field between gate and drain increases injection of carriers into substrate

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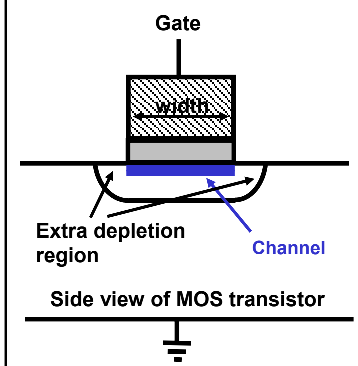
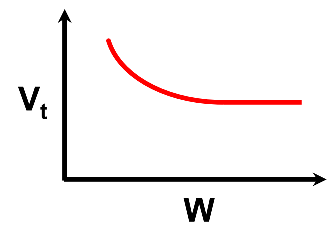
Narrow Width Effect

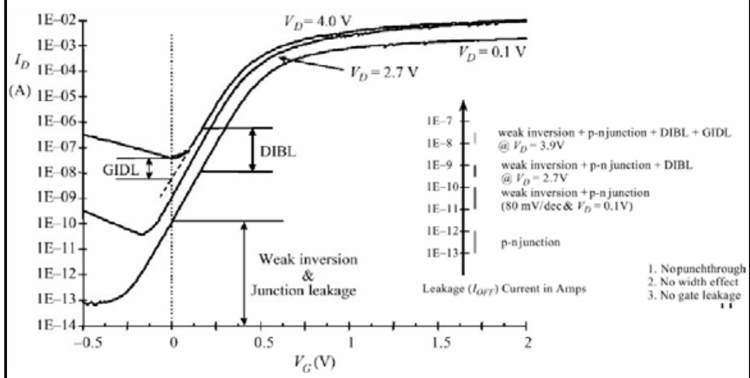


Side view of MOS transistor



- Depletion region extends outside of gate controlled region
- Opposite to V_t roll-off
- Depends on isolation technology

Leakage Components



[IEEE press, 2000]