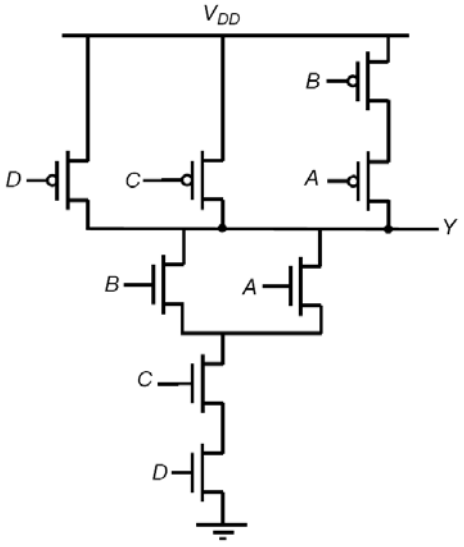
VLSI Design Homework #4
Static CMOS Circuits, midterm practice

1. Consider the circuit on the right

a. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8.

b. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

c. If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{DD}=2.5V, C_{out}=30fF and f_{clk}=250MHz.

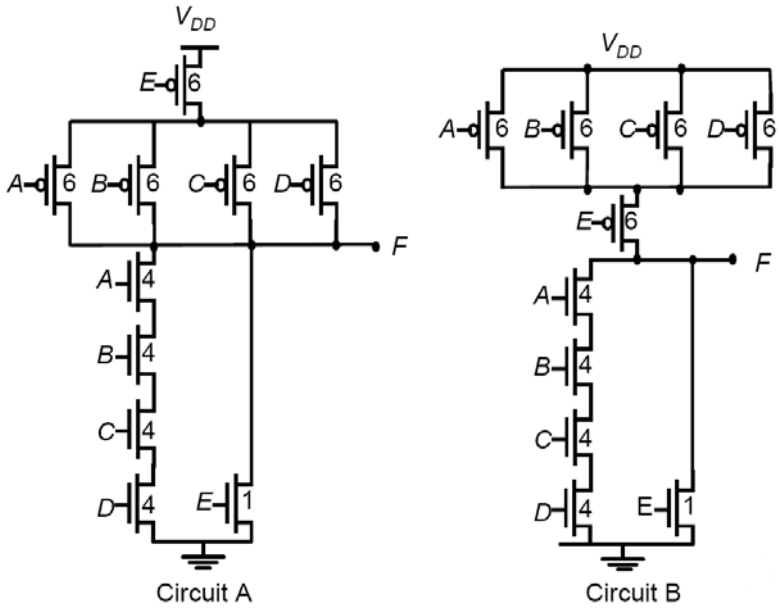


2. Consider the circuit to the right:

a. Do the following two circuits implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

b. Will these two circuits' output resistances always be equal to each other?

c. Will these two circuits' rise and fall times always be equal to each other? Why or why not?

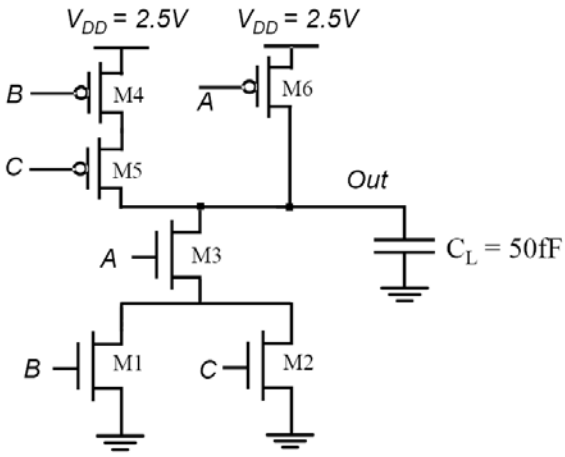


3. Consider the circuit below.

a. What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5μm/0.25μm.

b. Let the drain current for each device (NMOS and PMOS) be 1μA for NMOS at $V_{GS} = V_T$

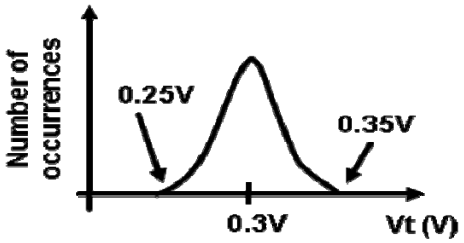
and PMOS at $V_{SG} = V_T$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL**.**



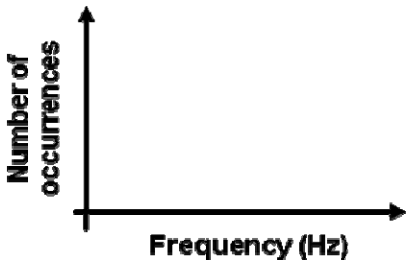
c. Suppose the circuit is active for a fraction of time *d* and idle for *(1-d)*. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr_{(A=1)}$ = 0.5, $Pr_{(B=1)}$ = 0.5, $Pr_{(C=1)}$ = 0.5) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle *d* for which the active power is equal to the leakage power? Use equation $I = I_0 e^{(V_{gs}-V_T)/0.1}$ for leakage calculation. Assume V_T=0.43.

4. [Process variation]

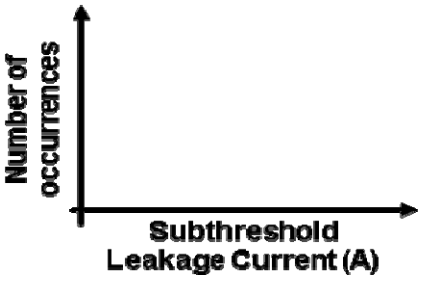
The statistical distribution of the MOSFET threshold voltage in a 45nm process is given in the left figure. It roughly follows a Gaussian distribution with a mean of 0.3V and a worst case variation of +/- 0.05V. Supply voltage is 1.0V, V_{dsat} is 0.3V, and subthreshold swing is 0.1V/dec. Assume these three parameters do not change with process variation.



(a) Sketch the statistical distribution of the circuit frequency for the given Vt variation. Calculate the ratio between the maximum and minimum frequencies.

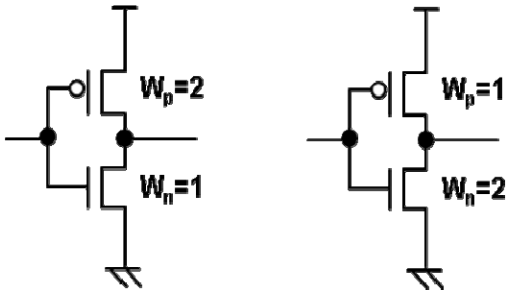


(b) Sketch the statistical distribution of the subthreshold leakage current (Vgs=0V) for the given Vt variation. Calculate the ratio between the maximum and minimum subthreshold leakage currents.



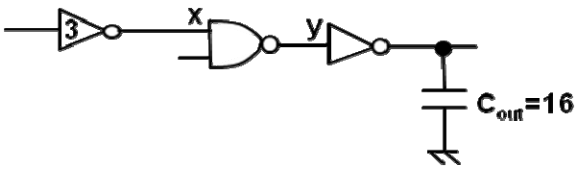
5. Circuit delay:

Consider two types of inverters. The left inverter has a balanced pull-up and pull-down while the right one has a skewed pull-up and pull-down. Which N-stage ring oscillator will run slower, one using balanced inverters or one using skewed inverters? What is the percentage difference between the balanced and skewed ring oscillator periods?



5. Sizing for speed

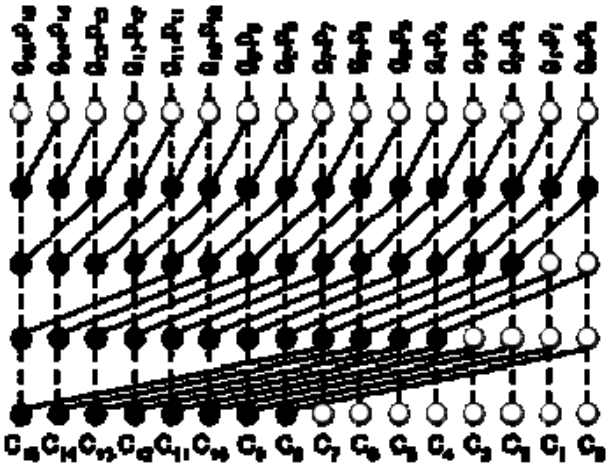
(a) Determine x and y for minimum delay.



Assume this is in a silicon-on-insulator process where $\gamma=0$ ($C_{int}=0$). For a static inverter, $W_P:W_N=2:1$ gives equivalent pull-up and pull-down resistance. Hint: You cannot directly apply the logical effort like we did in class because it does not hold for $\gamma=0$.

(b) When the input switches from 0V to V_{dd}, what is (i) the total energy drawn from V_{dd} and (ii) the total energy dissipated by heat?

Assume this is in a silicon-on-insulator process where $\gamma=0$ ($C_{int}=0$). The other input to the NAND gate is V_{dd}. Do NOT include the switching energy of the primary input. Use the x and y values calculated in part (a).



6 . در مدار جمع کننده Kogge-Stone روبرو دایره های سفید register هستند و دایره های سیاه شبیه عملگر دایره در Brent-Kung هستند:

a. مشخص کنید حاصل C10 چطور حساب میشود.
b. حداکثر تعداد عملیات برای به دست آوردن بیت ۱۰ و نیز بیت ۱۶ را در Kogge-Stone با Brent-Kung مقایسه کنید.
c. به چه دلیل تاخیر این جمع کننده میتواند از Brent-Kung کمتر باشد؟ به عبارت دیگر، چه مشخصه ای در Kogge-Stone هست که در Brent-Kung نیست؟