IUT - VLSI Design Homework #1
CMOS Inverter Schematic and Layout
Due by 22 Mehr (1 week)

Please go through the L-Edit/HSpice tutorials posted on the group discussion website and get familiar with the tools before starting the homework.

1. Draw the layout of a single CMOS inverter, and copy it three times so that each inverter drives the input of the next inverter. (Vdd=2.5V, .35μm CMOS process, 25°C, minimum channel lengths of .35μm, NMOS width=0.75μm, inverter cell height=150μm).
2. Simulate the high-to-low and low-to-high propagation delay of the designed inverter. Output of the inverter should be loaded with an identical inverter. Input of the inverter should be driven by an identical inverter to obtain a realistic (smooth) input waveform. For the input of the first inverter (driver), use a pulse with a rise/fall time of 0.03ns (tip: use "pwl" or "pulse" command in HSPICE to generate the input waveform).
3. Show how the high-to-low propagation delay changes as you vary the PVT (Process-Voltage-Temperature) parameters as follows. Analyze the results in a few sentences.
   A. Vth = +/- 10% (tip: change the VTH0 parameter in the device model file)
   B. Vdd = 2.25V, 2.5V, 2.75V
   C. Temperature = 0°C, 25°C, 110°C

[Deliverables]

1. Layout view of three inverters. Use the ruler to show the dimensions of the middle inverter
2. Netlist (spice) file for the layout
3. Waveforms of high-to-low and low-to-high propagation delays from post layout simulation. Mention the delay values in the plots.
4. Propagation delay values while varying PVT parameters.