
EE 5301 – VLSI Design Automation I

Part V: Placement

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References and Copyright

- Textbooks referred (none required)
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 - [She99] N. Sherwani
"Algorithms For VLSI Physical Design Automation"
Kluwer Academic Publishers, 3rd edition, 1999.

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References and Copyright (cont.)

- Slides used: (*Modified by Kia when necessary*)
 - [©Sarrafzadeh] © Majid Sarrafzadeh, 2001;
Department of Computer Science, UCLA
 - [©Sherwani] © Naveed A. Sherwani, 1992
(companion slides to [She99])
 - [©Keutzer] © Kurt Keutzer, Dept. of EECS,
UC-Berekeley
<http://www-cad.eecs.berkeley.edu/~niraj/ee244/index.htm>
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<http://www.ics.uci.edu/~rgupta/ics280.html>
 - [©Kang] © Steve Kang
UIUC
<http://www.ece.uiuc.edu/ece482/>

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Placement

- **Problem**
 - Given a netlist, and fixed-shape cells (small, standard cell), find the exact location of the cells to minimize area and wire-length
 - Consistent with the standard-cell design methodology
 - Row-based, no hard-macros
 - Modules:
 - Usually fixed, equal height (exception: double height cells)
 - Some fixed (I/O pads)
 - Connected by edges or hyperedges
- **Objectives**
 - Cost components: area, wire length
 - Additional cost components: timing, congestion

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Placement Cost Components

- **Area**
 - Would like to pack all the modules very tightly
- **Wire length (half-perimeter of the hnet bbox)**
 - Minimize the **average** wire length
 - Would result in tight packing of the modules with high connectivity
- **Overlap**
 - Could be prohibited by the moves, or used as penalty
 - Keep the cells from overlapping (moves cells apart)
- **Timing**
 - Not a 1-1 correspondent with wire length minimization, but consistent on the average
- **Congestion**
 - Measure of routability
 - Would like to move the cells apart

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Placement Algorithms

- **Top-Down**
 - Partitioning-based placement
 - Recursive bi-partitioning or quadrisection
 - Cut direction?
 - Partition vs. physical location
- **Iterative**
 - Simulated annealing
OR: Force directed
 - Start with an initial placement, iteratively improve the wire-length and area
- **Constructive**
 - Start with a few cells in the center, and place highly connected adjacent modules around them

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Simulated Annealing Placement

- **Cost**
 - Area (usually fixed # of rows, variable row width)
 - Wirelength (Euclidian or Manhattan)
 - Cell overlap (penalty increases with temperature)
- **Moves**
 - Exchange two cells within a radius R (R temperature dependent?)
 - Displace a cell within a row
 - Flip a cell horizontally
- **Low vs. High temperature**
 - If used as a post processing, start with low-temp
- **Post-processing?**
 - Might be needed if there are still overlaps

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Force-Directed Placement

- **Model**
 - Wires simulated as springs (if the only force, what will happen?)
 $Force_{ij} = Weight_{ij} \times distance_{ij}$
 - Cell sizes as repellant forces
 - [Eisenmann, DAC'98]:
"vacant" regions work as "attracting" forces
"overcrowded" regions work as "repelling" forces
- **Algorithm**
 - Solve a set of linear equations to find an intermediate solution (module locations)
 - Repeat the process until equilibrium

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Force-Directed Placement (cont.)

- **Model (details):**
 - Cell distances: either
 $\Delta x_{ij} = |x_i - x_j| \quad \Delta y_{ij} = |y_i - y_j|$
 - OR:
 $\Delta d_{ij} = (x_i - x_j)^2 + (y_i - y_j)^2$
 - Forces:
 $F_x^i = \sum_{j=1}^n (-k_{ij} \times \Delta x_{ij}) \quad F_y^i = \sum_{j=1}^n (-k_{ij} \times \Delta y_{ij})$
 - Objective: find x,y coordinates for all cells such that total force exerted on each cell is zero.

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Force-Directed Placement (cont.)

- **Avoiding overlaps or collapsing in one point?**
 - Use fixed boundary I/O cells
 - Use repelling force between cells that are not connected by a net
 - Do not allow a move that results in overlap
 - Use repelling "field" forces from congested areas to sparse ones [Eisenmann, DAC'98]

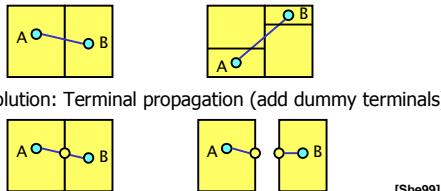
$$F_x^i = \left[\sum_{j=1}^n (-k_{ij} \times \Delta x_{ij}) \right] + E_x(x_i, y_i)$$

- **Problems with force directed:**
 - Overlap still might occur (cell sizes model artificially)
 - Flat design, not hierarchy

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Partitioning-based Placement

- **Simultaneously perform:**
 - Circuit partitioning
 - Chip area partitioning
 - Assign circuit partitions to chip slots
- **Problem:**
 - Circuit partitioning unaware of the physical location

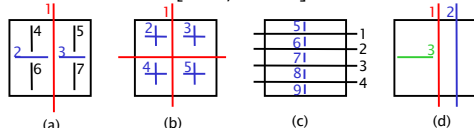


- **Solution:** Terminal propagation (add dummy terminals)

[She99] p.239
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Partitioning-based Placement

- **More problems:**
 - Direction of the cut? [Yildiz, DAC'01]



- How to handle fixed blocks? (area assigned to a partition might not be enough)
- How to correct a bad decision made at a higher level?

- **Advantages:**
 - Hierarchical, scalable
 - Inherently apt for congestion minimization, easily extendable to timing optimization

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To Probe Further...

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(force directed method)
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(quadrisection-based placement)

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To Probe Further...

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(cut directions in partitioning-based placement)
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"Runtime and Quality Tradeoffs in FPGA Placement and Routing",
International Symposium on Field Programmable Gate Arrays (FPGA),
pp. 29-36, 2001.
(placement and routing quality/speed trade-off)

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